The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte AKIHIKO KOH, TSUTOMU SAMPEI, NOBUHISA WATANABE
and AKIHIRO KIKUCHI

Appeal No. 2006-2407
Application No. 09/802,857

HEARD: October 17, 2006

Before THOMAS, RUGGIERO, and SAADAT, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION

Appellants have appealed to the Board from the examiner's final rejection of claims 13 through 25. Claims 1 through 12 have been canceled.

Independent claim 13 is reproduced below:

13. A data processing apparatus performing predetermined data processing in accordance with instruction codes read from a program memory storing a program, the data processing apparatus comprising:

a debugging circuit having a plurality of bug address setting registers and a plurality of coincidence detecting circuits,

one of said plurality of bug address setting registers holding one of a plurality of bug addresses that show the start of a buggy part of said program stored in said program memory,

one of said plurality of coincidence detecting circuits comparing a program address for reading instruction codes from said program memory with said one of said plurality of bug addresses held in said one of said plurality of bug address setting registers, said one of said plurality of coincidence detecting circuits outputting one of a plurality of coincidence signals when said program address and said one of said plurality of bug addresses coincide,

another of said plurality of bug address setting registers holding another of said plurality of bug addresses that show the start of another buggy part of the program stored in the program memory,

another of said plurality of coincidence detecting circuits comparing said program address for reading instruction codes from said program memory with said another of said plurality of bug addresses held in said another of said plurality of bug address setting registers, said another of said plurality of coincidence detecting circuits outputting another of said plurality of coincidence signals when said program address and said another of said plurality of bug addresses coincide; and

a central processing unit receiving said plurality of coincidence signals, wherein said central processing unit:

executes one of a plurality of debugging programs stored within random access memory when said one of said plurality of coincidence signals indicates a coincidence of said program address and said one of said plurality of bug addresses,

executes another of said plurality of debugging programs stored within said random access memory when said another of said plurality of coincidence signals indicates a coincidence of said program address and said another of said plurality of bug addresses, and

executes said program stored within said program memory when said plurality of coincidence signals indicates a non-coincidence of said program address and any of said plurality of bug addresses.

The following references are relied on by the examiner:

Sagane	5,454,100	Sep. 26, 1995
Hosotani	5,701,506	Dec. 23, 1997

Claims 13 through 25 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon Sagane in view of Hosotani.

Rather than repeat the positions of the appellants and the examiner, reference is made to the supplemental brief and reply brief for appellants' positions, and to the answer and supplemental answer (mailed on May 22, 2006) for the examiner's positions.

OPINION

As expanded upon here, we sustain the examiner's rejection of all claims on appeal under 35 U.S.C. § 103. Arguments are presented to us in the brief and reply brief only as to independent claim 13 and dependent claims 19 and 20. Therefore, the remaining dependent claims fall with our consideration of their parent independent claim 13.

Of the two embodiments in Sagane in figures 1 and 3, the examiner relies principally upon the showing in figure 3 which has been modified by the teachings in the paragraph bridging columns 6 and 7. The teachings there indicate the capability of the showing in figure 3 of processing sequentially a plurality of program bugs according to the structure set forth in figure 3 as well as the modified ability to process plural program bugs by plural key structural elements such as the comparator 8, the correction address register 21 and the correction data register 22. Although this teaching is not explicit as to the manner in which they would be interconnected with respect to the other elements in figure 3, it appears clear to the

artisan and to us that they would also be connected under a common bus environment as in figure 3 even as the discussion at the beginning of column 6 of Sagane as to the second embodiment in figure 3 relies in part upon the structural elements in the first embodiment in figure 1. These in turn are further modified according to the additional teaching at the top of column 7 of the need or proposal of an additional modification of the second embodiment to interpose a control flag switch 7a and switch 7c of figure 1 between the comparator 8 and the switch 23 in the figure 3 or second embodiment. This appears to relate to the additional modification of duplicated structures just mentioned to accommodate the sequential switching between a plurality of bugs in the program.

Before we treat the teachings in Hosotani, independent claim 13 on appeal does not require that the central processing unit receive the plurality of coincidence signals at the same time. Thus, the claim is consistent with the teaching value of Sagane of the ability as modified according to the just-noted teachings of the figure 3 embodiment to accommodate sequentially separate bugs. Implicit with this understanding then is the ability of the system to generate a plurality of different

time sequence signals to be switched by switch 23 to the data bus 5 which feeds directly to the CPU 2 in figure 3. Thus, in Sagane the duplicated structural elements noted earlier would perform a sequential execution of a plurality of debugging programs upon the respective coincidence signals detected by the plural comparators by their issuance of the coincidence or matching signal A in figure 3. If there is no coincidence, the program executes in a normal fashion as required at the end of claim 13 on appeal.

Notwithstanding the arguments in the brief and reply brief urging the conflict between the interrupt generation approach in figure 1 of Sagane and the absence of this in figure 3, there is no requirement of independent claim 13 on appeal of any interrupt being generated or required by the circuit elements claimed. Notwithstanding this observation about the actual recitations in claim 13, within 35 U.S.C. § 103 it appears clear to us that the artisan would have recognized that the circuitry in figure 3 functions in a manner consistent with the CPU receiving an interrupt-type switching of the sequencing of the program as would be expected in a

normal interrupting environment. Because the CPU 2 in figure 3 of Sagane would effectively bypass its normal program sequencing to eliminate the program bug within its normal programming in ROM 3 upon the normal operation of the plurality comparators 8 in figure 3, the effect of the operation of the system in figure 3 is to function in a manner analogous to an interrupt as directly taught in the embodiment in figure 1 of Sagane. In this manner, the functional analogy of Sagane is consistent with the broad recitation of dependent claims 19 and 20 that Sagane would effectively receive the plurality of coincidence signals "as" a single or plural/separate interrupts, since Sagane has the capability to perform both according to the modified teachings of figure 3 to accommodate plural bugs.

We agree as well with the examiner's remarks at least at pages 4 through 6 of the answer that the mere reception of the coincidence signals by the CPU of claim 13 does not require explicitly a direct connection or a direct coupling. We therefore agree with the examiner's indirect coupling or indirect connectability arguments in the answer.

The teachings of Hosotani are also compelling of the obviousness of the claimed subject matter. The most pertinent figures appear to be those in figure 2, 4, 6 and 10. There is also an explicit statement at column 4, lines 57 through 59 to be able to correct plural system bugs. The operation of the OR gate in these figures which results from a match circuit/coincidence circuit output from subcircuits 9a-9c, as well as the operation of the switch/connection control 10, provides a selective output from one or plurality of bugs detected to the data bus 5 which feeds directly to the CPU 1 in figure 2, for example, of Hosotani. The effective functionality of this reference appears to be consistent with the modified teachings of the second embodiment showing in figure 3 of Sagane.

Appellants' remarks at pages 11 and 12 of the principal brief on appeal therefore do not argue against the combinability of Sagane and Hosotani within 35 U.S.C. § 103. Notwithstanding this observation anyway, it appears to us that the artisan would have found it obvious to have combined the teachings of both references within 35 U.S.C. § 103 to provide an optimized approach to addressing the situation of a plurality of bugs in a programming sequencing operation for a CPU.

We also note briefly appellants' remarks at page 11 of the principal brief on appeal alleging the examiner has exercised an obvious-to-try rationale. The arguments actually have not been developed, but merely asserted. We therefore do not agree with appellants observation that the examiner has exercised a prohibited obvious-to-try analysis in formulating the rejection of the claims on appeal. We simply do not see that the evidence provided by the examiner and the rationale of combinability is consistent with a prohibited obvious to try rationale. In re O'Farrell, 853, F2.d 894, 903, 7 USPQ2d 1673, 1681 (1988) indicates that an obvious to try rationale is permitted within 35 U.S.C. § 103 as long as the prior art provides a reasonable expectation of success, while not providing only general guidance or the varying of all parameters or trying each of a significant number of possible choices until one arrived at the claimed invention. Obviousness does not require absolute predictability of success.

In view of the foregoing, the decision of the examiner rejecting all claims on appeal under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR §1.136(a). See 37 CFR § 1.136(a)(1)(iv).

AFFIRMED

JAMES D. THOMAS)
Administrative Patent Judge)
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JOSEPH F. RUGGIERO) BOARD OF PATENT APPEALS
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